Atomic layer deposition (ALD)

We carry out ALD processes on wafer, batch and chip level with four different ALD tools.

**ALD mini (PICOSUN® R-200 std.)**
- R&D of new materials
- Can be loaded manually with 200 mm wafers as well as any wafer and chip size below Ø 200 mm

**ALD cluster (PICOSUN® R-200 adv.)**
- Allows automatic handling and successive processing of 25 wafers of 200 mm
- Two chambers are designed respectively for thermal ALD and plasma-enhanced ALD

**ALD batch (PICOSUN® P-300B)**
- 25 wafers of 200 mm can be processed simultaneously with homogeneous quality, aiming for a high throughput

**F.A.S.T.-ALD (Plasma-Therm F.A.S.T.8)**
- Four-chamber system specialized for TSV and µVia production necessary for wafer stacking
- The automatic handling of 200 mm wafers is configured to process a whole 25 wafer batch successively

Technology Services

Fabrication of demonstrators and prototypes up to pre-production and pilot production.
- Automated, cassette-to-cassette equipment set up for 200 mm wafers (8“)
- Area ISO4 cleanroom: >1000 m² ISO 9001 certified management system since 1995
- Digital production using modern Manufacturing Execution System (MES) by CM
- Comprehensive system for process monitoring
- Integration of wafers from external foundries
- Capacity: 4500 wafers per year
- Member of the Research Fab Microelectronics Germany (FMD)

Fraunhofer IMS

Working on a safe, secure and sustainable future with the help of Smart Sensor Systems:

Our institute consists of numerous research labs, in which we provide ASIC and chip design, CMOS, MEMS, LiDAR development services and many more microelectronic solutions. A seamless path from initial idea to development and production, while maintaining the highest quality and reliability standards, is our offer.

We look forward to giving a long-term support to our customers and be a reliable research and development partner. Fraunhofer IMS provides numerous technologies in four business units: Health, Industry, Mobility, as well as Space and Security.
Customizable photonics platform

We offer services to support your idea at all stages from first draft to pilot fabrication. Our services include:

- Device design and simulation
- Process development
- Chip fabrication to pilot fabrication
- Device characterization
- Process transfer

Our technology platform is accessible via R&D collaborations and contracting. We are also open to collaborative projects with public funding.

Post-CMOS photonic platform

Our Post-CMOS compatible SiN-photonics platform offers low-loss components with a broad choice of device geometries and user-defined customization options.

Fraunhofer IMS platform offers silicon-nitride photonics and options for integration of new materials. Our platform uses back-end-of-line processes to enable photonics as a post-processing option on foundry wafers containing CMOS circuitry.

Based on our extensive combined experience in integrated circuits, Post-CMOS sensors and photonics, we guide you from first idea to prototype and ramp-up.

Process chain technologies

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<td>Converting all necessary layers into an adequate layout Transferring alignment marks and test structures</td>
<td>0.35 µm resolution 8&quot; Wafer Stepper 8&quot; Mask Aligner Backside-Alignment possible Stitching</td>
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<tr>
<td>Etching</td>
<td>Sacrificial layer technology</td>
<td>Wet chemical DRIE Ion Beam Milling / Etching Isotropic release etch (XeF2, HF) Plasma enhanced etching</td>
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<td>CMOS single photon Avalanche diodes (CSPAD) detector for light imaging, detection, and ranging (LiDAR) Electrical wafer-to-wafer connection through microvias</td>
<td>Wafer thinning Wafer-to-wafer-bonding Chip-to-chip-bonding Chip to wafer bonding Through Silicon Vias (TSVs) 8&quot; Wafer</td>
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<td>Metrology</td>
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<td>Void inspection Electrical wafer testing Surface profiling Sheet resistance Layer thickness, CD, and Overlay measurements Chip to wafer Through Silicon Vias (TSVs)</td>
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