Atomic layer deposition (ALD)

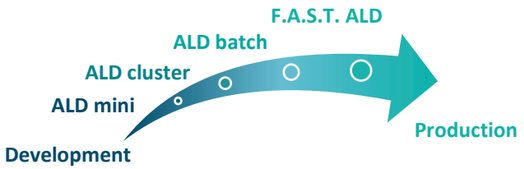
We carry out ALD processes on wafer, batch and chip level with four different ALD tools.

ALD mini
- R&D of new materials
- Can be loaded manually with 200 mm wafers as well as any wafer and device size below Ø 200 mm

ALD cluster
- Allows automatic handling and successive processing of 25 wafers of 200 mm
- Two chambers are designed respectively for thermal ALD and plasma-enhanced ALD

ALD batch
- 25 wafers of 200 mm can be processed simultaneously with homogeneous quality, aiming for a high throughput

F.A.S.T.-ALD
- Four-chamber system specialized for TSV and µVia production necessary for wafer stacking
- The automatic handling of 200 mm wafers is configured to process a whole 25 wafer batch successively



ALD support for every step from precursor- and process development to pilot production.

Contact

Technology Services
sales@ims.fraunhofer.de

Fraunhofer Institute for Microelectronic Circuits and Systems IMS
Finkenstraße 61
47057 Duisburg
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Fraunhofer IMS

Fraunhofer Institute for Microelectronic Circuits and Systems IMS

Covering the full process chain

Technology Services

Technology Services

Fabrication of demonstrators and prototypes up to pre-production and pilot production.

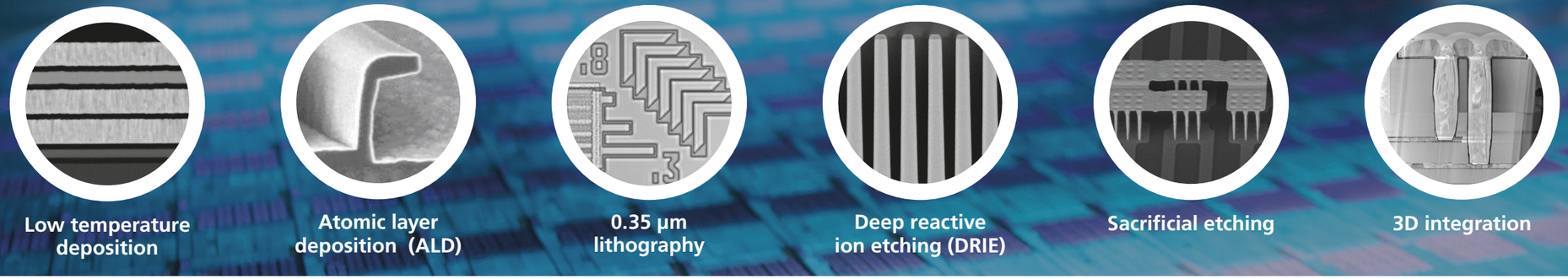
- Automated, cassette-to-cassette equipment set up for 200 mm wafers (8“)
- Area ISO4 cleanroom: >1000 m²
- ISO 9001 certified management system since 1995
- Digital production using modern Manufacturing Execution System (MES)
- Comprehensive system for process monitoring
- Integration of wafers from external foundries
- Capacity: 4500 wafers per year
- Member of the Research Fab Microelectronics Germany (FMD)

Fraunhofer IMS

Working on a safe, secure and sustainable future with the help of Smart Sensor Systems:

Our institute consists of numerous research labs, in which we provide ASIC and chip design, CMOS, MEMS, LiDAR development services and many more microelectronic solutions. A seamless path from initial idea to development and production, while maintaining the highest quality and reliability standards, is our offer.

We look forward to giving a long-term support to our customers and be a reliable research and development partner. Fraunhofer IMS provides numerous technologies in four business units: Health, Industry, Mobility, as well as Space and Security.



From idea to platform

Our services to support your photonic integrated circuit idea at all stages: from first draft to pilot fabrication.

Our services include:

- Device, system design and simulation
- Process development
- Chip fabrication to pilot fabrication
- Device characterization
- Process transfer

Our technology platform is accessible via R&D collaborations and contracting. We are also open to collaborative projects with public funding.

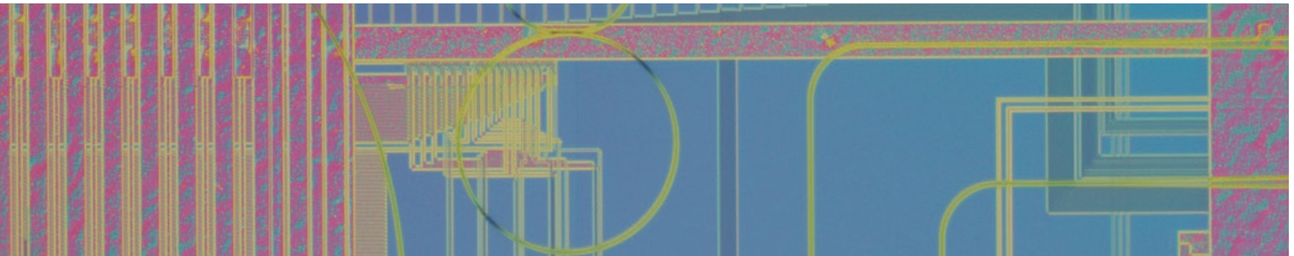
Post-CMOS photonic platform

The Fraunhofer IMS post-CMOS compatible SiN-photonics platform offers low-loss components with a broad choice of device geometries and customized options.

Our photonics platform includes integration options of new materials. We use back-end-of-line processes to enable direct interation of photonics on CMOS wafers.

The dielectric waveguide materials support a broad range of wavelengths from 370 nm - 3 µm. Layers thicknesses and material types can be customized.

Photonics and electronics made on one manufacturing platform.



Process chain technologies

Process step	Application examples	Specification
Deposition	■ Functional / sensitive layers ■ Isolating / conductive layers ■ Layer stack for biomedica encapsulation via ALD ■ Temperature sensitive applications	■ CVD: SiO, SiN, Si (B, P, Ge), Ge, aSi, B, W ■ PVD: Ti/TiN, TiW, Cu, AlSi, AlCu ■ ICP: aSi, SiO, SiN, DLC ■ ALD: Al_2O_3, Ta_2O_5, ZnO, AZO, TiAlCN, TiN, Ru, MoS_2, WS_2, SiO_2, Cu ■ Thermal: SiO_2
Lithography	■ Converting all necessary layers into an adequate layout ■ Transferring alignment marks and test structures	■ 0.35 µm resolution ■ 8“ Wafer Stepper ■ 8“ Mask Aligner ■ Backside-alignment possible ■ Stitching
Etching	■ Sacrificial layer technology ■ Etching of deep holes / trenches	■ Wet chemical ■ DRIE ■ Ion Beam Milling / Etching ■ Isotropic release etch (XeF_2, HF) ■ Plasma enhanced etching

Process step	Application examples	Specification
3D integration	■ CMOS single photon avalanche diodes (CSPAD) detector for light imaging, detection, and ranging (LiDAR) ■ Electrical wafer-to-wafer connection through microvias	■ Wafer thinning ■ Wafer-to-wafer-bonding ■ Chip-to-chip-bonding ■ Chip-to-wafer bonding ■ Through Silicon Vias (TSVs) ■ 8“ Wafer
Metrology and test	■ Scanning acoustic microscopy to detect voids at the interface between two bonded wafers ■ Electric characterisation ■ Electro-optical characterisation	■ Void inspection ■ Electrical wafer testing ■ Surface profiling ■ Sheet resistance ■ Layer thickness, CD, and overlay measurements ■ Chip to wafer ■ Through Silicon Vias (TSVs)