Fraunhofer IMS

Fraunhofer Institute for Microelectronic Circuits and Systems IMS

CMOS-Compatible Solutions for Scalable Trapped-Ion Quantum Computing

Harnessing Light: Enabling Quantum Potential

At Fraunhofer IMS, we support the development of quantum computing by leveraging our deep expertise in CMOS-compatible electronics and integrated photonics.

By building quantum technologies on proven CMOS processes, we help make them more scalable and ready for practical use. Because integration is key!

With over 30 years of experience in CMOS development, Fraunhofer IMS offers a CMOS-compatible 8-inch production line built to industry standards.

Scalability is essential for bringing quantum computing into real-world applications. Trapped-ion systems are one of the leading approaches in this field — but they require integrated detection solutions to truly scale.

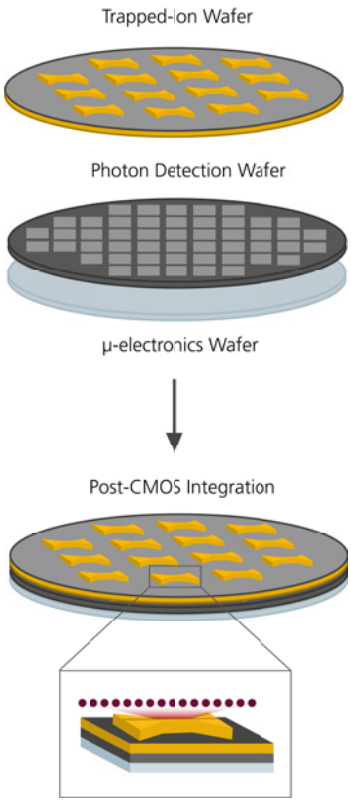
That's where we come in: Fraunhofer IMS develops integrated, CMOS-compatible systems that combine detection, photonics, and readout electronics in a single solution. Whether through monolithic or hybrid integration, we offer an all-in-one approach to help advance quantum technologies.

Customizable Sensitivity

- **CMOS-Compatible Integrated Approach:** Leveraging 35 years of expertise to support the development of quantum technologies
- **3D Integration Techniques:** Seamlessly combining SPAD functionality with readout microelectronics and integrated photonics
- **One-Wafer Processing:** Utilizing our industry-standard clean room for streamlined concept-to-demonstration solutions
- **Tailored Solutions:** Custom designs to meet specific quantum technology requirements
- **Collaborative Research:** Partnering with industry leaders to drive quantum innovation forward

SPADs for Harnessing Light

- 0.35 µm CMOS Opto-Process for SPAD fabrication
- Readout ICs implemented in standard CMOS Process (e.g. 0.18 µm)
- Low Dark-Count Rate: 6.5 cps/µm²
- High Photon Detection Probability 60% @ 550 nm (70% @ 370 nm under development)
- Wavelength sensitivity tuning [200 nm, 1000 nm]
- Signal-to-Noise ratio optimization and Low Light Imaging



Post-CMOS integration of trapped-ion wafers with photodiodes and Read-Out Integrated Circuits (ROIC) for signal processing.

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Integrated SPAD

CMOS SPAD Array for Quantum Technologies

	Value	Unit
Technology	0.35 µm CMOS (SPAD), Backside-Illumination, 3D Integration, W2W Bonding, ROIC on 8" wafer	
Dark Count Rate	6.5	cps/µm²
Photon Detection Probability	370 nm: 70[1] (under development)	%
	550 nm: 60[1]	%
Operating Temperature	300 - 100 (tested)	K
	100 - 10 (under development)	K
Breakdown Voltage	34	V
Operation Voltage	40	V
Fill Factor	without MLA 9.6	%
	with MLA > 90	%
SPAD Pixel Size	40 x 40	µm
SPAD Diameter	14	µm
Dead Time	20	ns
TDC Resolution (e.g. from LiDAR application)	312.5	ps

[1]Simulation results

Contact and further information

sales@ims.fraunhofer.de

Fraunhofer Institute for Microelectronic Circuits and Systems IMS
Finkenstraße 61
47057 Duisburg