

Fraunhofer Institute for Microelectronic Circuits and Systems IMS

Photonic waveguides

Customizable Post-CMOS photonics platform

From idea to pilot fabrication

The Fraunhofer IMS Post-CMOS photonic platform uses a state of the art in house cleanroom, utilizing advanced automated systems for 8" wafer processing. This platform offers customizable processes tailored to meet specific application requirements, drawing on over 35 years of extensive microelectronic experience at the production level.

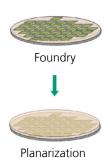
It facilitates the monolithic integration of photonics and electronics, ensuring seamless compatibility with Post-CMOS technologies. The platform employs sophisticated Post-CMOS temperature budget processing methods, allowing for precise thermal management during fabrication. The photonic layer stack, which includes essential components such as waveguides, heaters, and cladding, is deposited in a manner that maintains full compatibility with CMOS standards. Additionally, the platform is flexible and can accommodate the integration of various materials upon request, providing a versatile solution for diverse photonic applications.

Highly customizable waveguides

- Main waveguide platform: Silicon nitride (Si_xN_y) and "PE VIS" (Si_xN_y with optimized transmission for visible wavelengths) via plasma enhanced chemical vapor deposition (PECVD)
- Waveguide thicknesses: 20 nm to 800 nm
- Minimum feature size: 250 nm (deep UV lithography stepper)
- Other waveguide platforms: Si₃N₄ by low pressure chemical vapor deposition (LPCVD), tantalum pentoxide (Ta₂O₅) by atomic layer deposition (ALD), aluminium nitride (AlN) by sputtering

Low-loss waveguides

- Waveguides characterized for VIS and NIR wavelengths
- The results of the measured waveguide attenuation are in alignment with the established standards of foundries
- Ring resonators and Mach-Zehnder inteferometer are available as passive building blocks. The devices can be tuned via thermo-optical heaters







Post-CMOS integration

Post-CMOS waveguide integration begins with CMOS wafer planarization and deposition of a bottom oxide layer, followed by integrating photonic waveguides on the top

