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RISC-V Processor for Embedded AI applications

AIRISC - RISC-V CORES

Fraunhofer Institute for Microeletcronic Circuits and Systems IMS

Finkenstr. 61
47057 Duisburg
phone: +49 203 37 83-0
www.ims.fraunhofer.de
www.airisc.de

RISC-V Ambassador
Alexander Stanitzki
alexander.stanitzki@ims.fraunhofer.de

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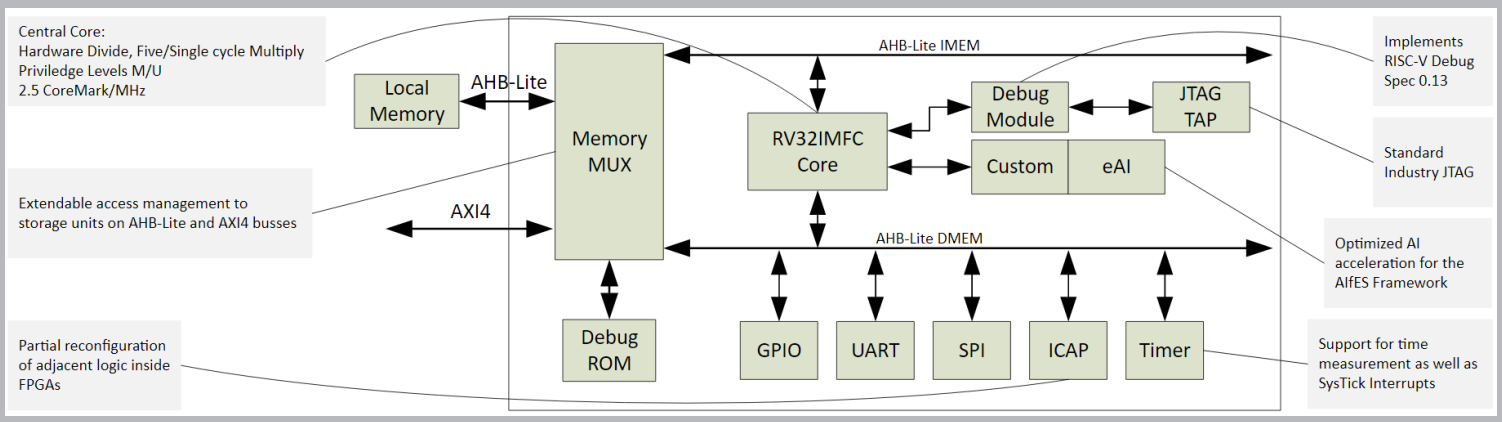
Trustworthy RISC-V Cores

The AIRISC family of RISC-V cores from Fraunhofer IMS enables efficient machine learning and AI in sensors, IoT devices and other embedded applications.
AIRISC variants with extended safety mechanisms such as dual core lock-stepping (DCLS) or error correcting codes (ECC) are available for use in fail-safe systems according to ISO 26262 (up to ASIL-D) and DIN 61508. Since intellectual property protection is highly relevant in these applications, the AIRISC family offers functions for cryptographic security, such as firmware protection and secure boot.
The free RISC-V architecture makes it possible to implement customer-specific extensions in a short time and thus provide optimum computing performance futzor special applications. These features make AIRISC the best choice for real-time embedded sensor applications and integration into IoT systems.

Designed for Embedded AI

In interaction with the AIfES software library invented by Fraunhofer IMS, the AIRISC processor family supports the inference and training of neural networks directly on the embedded device. Integrated accelerators enable distributed training in networked devices (federated learning) and also the calibration of sensors using AI. Image processing directly in the sensor, without the need for permanent communication with the cloud, makes the AIRISC processor interesting for energy-autnomous and wearable sensor systems.



Block diagram AIRISC

Features

- 32-bit, 5-stage pipeline
- Highly modular: tune area, power and performance by enabling features in a single central configuration file
- E - reduced register set
- M - single cycle multiplier/divider
- C - compressed instructions
- F - single precision floating point unit (FPU)
- Branch prediction and Return Address Stack (RAS)
- Configurable hardware breakpoints/watchpoints
- Hardware support for AIfES embedded AI library

Modules/Peripherals

- AHB-Lite system interface
- GPIO
- UART
- SPI Master/Slave
- Timer
- JTAG
- Dynamic reconfiguration module (on Xilinx 7-series)

Deliverables

- RTL verilog sources
- Verification suite
- Synthesis and P&R scripts for Cadence Genus/Innovus
- Register and module description
- Integration guide
- Example projects for Diligent NexysVideo, CMOD A7 and Arty A7 boards
- Including Coremark, FreeRTOS-Demo, Peripheral Demo and embedded AI Demo

Design Support and Customization for FPGA and ASIC available.
Silicon proven in 180 nm and 65 nm technology.

Size and Performance

Measured values and simulation results:

Process / Device	Configuration	LUT/FF or Area in mm²	$f_{clk,max}$ in MHz	Energy Consumption in uW/MHz
XFab XH018	RV32IMC	0,68 mm² (excl. SRAM)	48	
TSMC N65	RV32IMC	0,14 mm² (excl. SRAM)	350	
	RV32IMFC	0,28 mm² (excl. SRAM)	>100	53
Artix7 A200T (Nexys Video)	RV32EC	2930 (2.19 %) / 1524 (0.57 %)	32	
	RV32IMC	4598 (3.44 %) / 2606 (0.97 %)	32	
	RV32IMFC	8189 (6.12 %) / 4305 (1.61 %)	32	
Artix7 A35T (Arty A7)	RV32EC	2928 (14.08 %) / 2605 (6.26 %)	32	156.2
	RV32IMC	4595 (22.09 %) / 2605 (6.3 %)	32	
	RV32IMFC	8182 (39.34 %) / 4304 (10.35 %)	32	437.5