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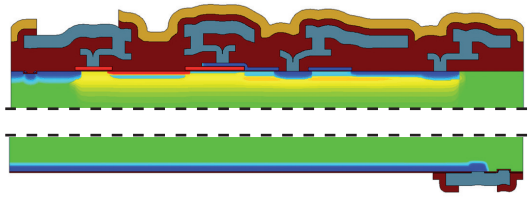

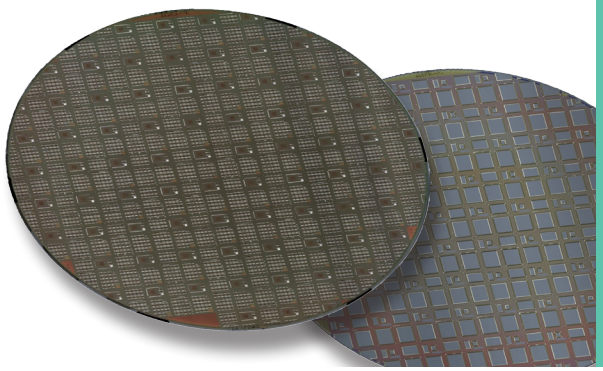

1 *Simulated cross section of double-sided CMOS process*
2 *Frontside and backside of a double-sided processed wafer*
3 *Four metallization layers with planarized passivation*
4 *Color filters*

ENHANCED CMOS FOR OPTICAL SENSORS AND DETECTORS

Optical sensors based on CMOS technologies have reached a level that exceeds the performance and quality of established CCD sensors. The development of specific photodetector components or special processing of the silicon surface has notably improved device attributes. As a competent and reliable provider of microelectronic devices and technologies, IMS offers customized solutions in particular for photo detectors and image sensors. By adapting and extending standard 0.35 µm CMOS technology, IMS fulfils specific sensor requirements such as spectral sensitivity or quantum efficiency. For example sensitive Single Photon Avalanche Diodes (SPAD) with customer specific properties (e. g. breakdown voltage) or "Opto" modules (e. g. UV transparent passivation) are possible. IMS CMOS technology not only offers a variety of optical devices but also the possibility of on-chip integration with the individual read-out circuit. With the aid of special processes, such as a planarized passivation, the integration of additional features like optical filters is enabled.

Deep optical stack etching

Variations of spectral sensitivity can be caused by interferences due to the complex stack of inter-metal dielectrics in the wiring of image sensors. Eliminating these variations is crucial for applications using narrow-bandwidth illumination or relying on quantitative measure-ments. By deep optical stack etching, IMS removes these variations and also extends sensitivity to the extreme UV range.

Double-sided CMOS processing

The wiring of pixel arrays and integrated read-out circuitry reduce the detected amount of light. Especially, for small pixel sizes and good low-light performance, backside illumination can strongly improve sensor properties. Whereas backside illumination often is realized by post-processing of single-sided CMOS wafers, IMS has developed methods to implement CMOS

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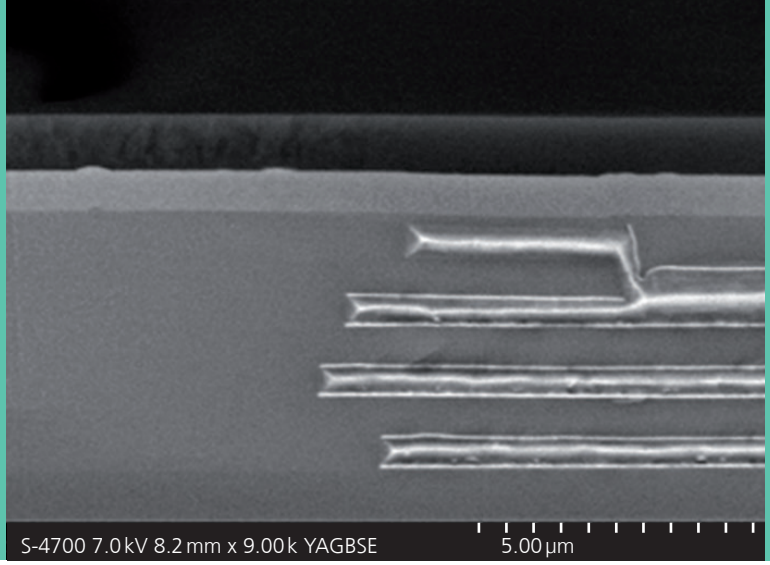

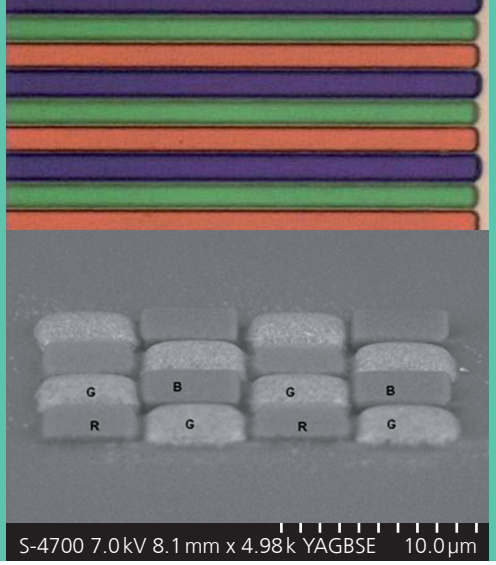

processing on both wafer sides. This enables the realization of backside illuminated sensors as well as fully depleted detectors.

SOI-CMOS processing for backside illuminated sensors

Especially for pixels with complex data-processing within the pixel, like actively-quenched Single Photon Avalanche Diodes (SPADs), high fill factors are difficult to achieve. Therefore, IMS has developed a backside illuminated SPAD technology (BackSPAD) based on a 0.35 µm SOI-CMOS process. The wafer containing readout circuitry is fabricated in a standard CMOS technology and bonded to the detector array SOI- wafer. Afterwards, the complete handle-wafer or a window is removed to enable backside illumination. Depending on the specific process flow additional steps for anti-reflective coating (ARC) and microlenses are possible.

Planarized interfaces for color filters and microlenses

With the aid of the IMS microsystem cleanroom (MST-Lab&Fab) additional functionalities can be integrated on top of the passivation, such as tunable filters or microlenses. The integration of microlenses or color filters directly on top of the sensor chip is an efficient way to increase fill factor or realize color sensitive pixels. Microlenses enable a reduction of pixel size without decreasing the signal to noise ratio.

With customized CMOS technology IMS realizes your individual sensor concept – from first idea to pilot production.

Technological parameters

Wafer size:	200 mm
Chip size:	Up to 2 cm x 2 cm; larger sizes up to full-wafer chip possible with stitching
Critical dimensions:	down to 0.35 µm
"Opto" modules:	UV-transparent passivation (sensitivity down to 200 nm) Planarized passivation
Backside processes:	Ion implantation, contact and metal structuring, passivation, structuring of entrance window
Alignment accuracy:	≤ 1 µm (frontside to backside)
Post-processing:	Microlenses, color filters, tunable filters, anti-reflective coating Flip bonding (chip-to-chip, chip-to-wafer or wafer-to-wafer)

Advantages

- Fast fabrication times in an automotive-qualified CMOS cleanroom
- Individual support for your project (feasibility study, simulation, process and device development, fabrication, characterization, qualification, process transfer)

Applications

- Frontside (FSI) and backside (BSI) illuminated sensors
- Fully depleted sensors (e. g. photon counting, x-ray imaging)
- Single Photon Avalanche Diodes (SPAD)
- 3D sensor integration