



- 1 *Chip-to-wafer process for infrared sensors*
- 2 *Chip-on-board installation of a CSP*

CHIP SCALE PACKAGES FROM IMS

EXTREMELY SMALL, EXTREMELY GOOD

Fraunhofer Institute for Microelectronic Circuits and Systems IMS

Finkenstr. 61
D - 47057 Duisburg
phone +49 203 37 83-0
fax +49 203 37 83-266
www.ims.fraunhofer.de

contact
Michael Bollerott
phone +49 203 37 83-227
vertrieb@ims.fraunhofer.de

The triumph of microelectronics is based largely on two pillars – miniaturization of structure and price-cutting. This applies to silicon chips as well as to their packaging: from the dual in-line packages of the 1970s and 80s to SMD technology up to the smallest packaging possible – chip scale packages (CSP).

Fraunhofer IMS has developed a CSP for client-specific microsystems, for example MEMS resonators or accelerometers. It offers significant advantages over conventional packages made of metal, plastic or ceramics:

- It is only slightly bigger than the chip itself.
- It allows sensors to be operated in vacuum or inert gas.
- It is cost-effective and it can be produced in quantity.

- It is made of silicon and therefore provides excellent thermal properties.

At Fraunhofer IMS the CSP is deployed for infrared sensors produced on-site. In this case, the demands on the CPS regarding vacuum and tightness (leak rate) are particularly high.

The exceptional reliability of the CSP has been evidenced by tests such as autoclave, temperature load alternation and storage.

Example for a CSP with vacuum

Lid size	10 mm x 10 mm
Cavity volume	< 8 μ l
Cavity pressure	< 10 μ bar
Leak rate	< 1×10^{-15} mbar l/sec





CSP process

This CSP can be applied to other microsystems. The complete production on 200 mm wafers is carried out at Fraunhofer IMS. Regarding the preferred chip-to-wafer (C2W) process, only approved devices (known good die) are encapsulated, thereby reducing process time and material cost – this is important especially concerning large chip areas.

On the whole, there are great advantages arising from the production in the C2W

process, since the automatized characterization of the microsystem and of the CSP is possible after every process step.

The lid and the substrate wafers can be optimized independently. For example, antireflective coatings or optical multilayers for filtering certain wavelengths (cut-on filter) provide a more accurate measuring method. The use of glass as lid material is also possible.

Fraunhofer IMS offers the complete development of CSP processes for different microsystems, which can be implemented on request either as prototype or as small batch.

Further Parameter of the CSP process

Lid sizes	1 mm - 20 mm
Distance between lid and substrate	10 μm - 30 μm
Metals by electroplating	Cu, Sn, Ni, Au
Stacking method	C2W or Wafer-to-wafer (W2W)
Fixation technique	Thermocompression
Accuracy of placement	$\pm 0,5 \mu\text{m}$
Soldering temperature	250 °C - 350 °C
Soldering process	Solid liquid interdiffusion