



**Fraunhofer**  
IMS

FRAUNHOFER INSTITUTE FOR MICROELECTRONIC CIRCUITS AND SYSTEMS IMS

## **MICROSYSTEMS TECHNOLOGY LAB&FAB**



# YOUR IDEA – WE WILL REALIZE IT

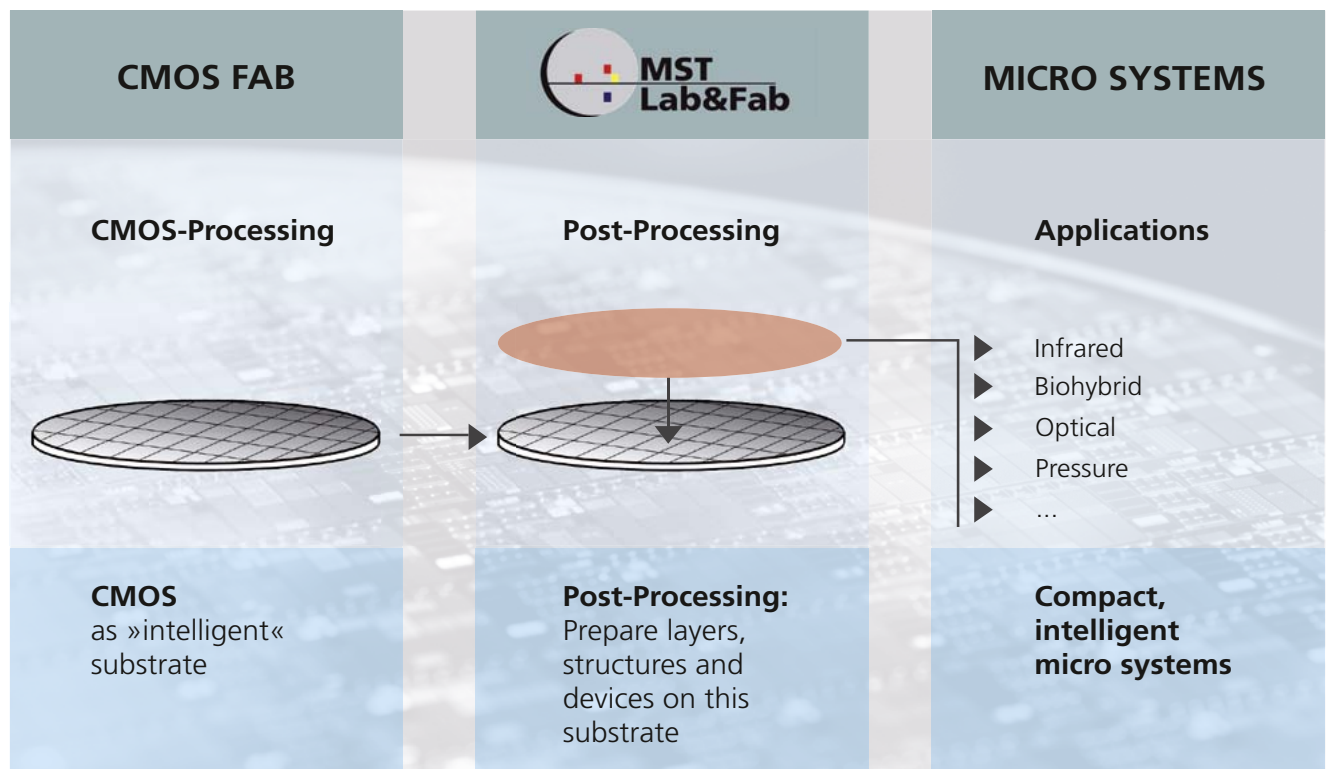
## Your product idea

It starts with your idea or your vision of a new product. You may be uncertain about feasibility, costs, potential risks or the technology which leads to the optimal product. As a research and development institute of the Fraunhofer-Gesellschaft, we offer you advice and support.

We accompany your project with concept and feasibility studies from the very start – from the specification and the design to the draft and the fabrication of prototypes through to the product qualification.

The pilot fabrication of your circuits and ICs is carried out by us as well. At our institute you receive microelectronics from a single source.

We provide our services and know-how across all industries. Our circuits and systems are used in particular when it comes to the creation of unique selling points and competitive advantages for our customers. Thus our customer is able to serve his target market in an optimal way.



### Step by step to project success

The way to a successful project is work-intensive and requires a good planning. Step by step, the following project phases are passed through:

- Concept & feasibility studies
- Specification & design
- Demonstrator development
- Prototype development
- Qualification
- Pilot fabrication

### Quality pays off

The Fraunhofer IMS is certified according to DIN EN ISO 9001 since 1995. The certificate is valid for all divisions of the institute: Research, development, production and distribution of microelectronic circuits, electronic systems, microsystems and sensors as well as consulting in these fields. The CMOS line is certified according to ISO/TS 16949.

The success of your project is our mission.

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### Infrastructure

#### Microsystems Technology Lab&Fab

Wafer size	200 mm (0.35 $\mu\text{m}$ )
Cleanroom area	600 m <sup>2</sup>
Cleanroom class	10
Capacity	5.000 wafers/year

#### CMOS factory

Wafer size	200 mm (8 inches, 0.35 $\mu\text{m}$ )
Cleanroom area	1,300 m <sup>2</sup>
Cleanroom class	10
Employees	150 in 4 shifts
Capacity	> 70.000 wafers/year



# CAPABILITIES

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## Substrates

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Size	200 mm / 8 inches
Material	Si, SOI, others on demand

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## Intelligent Substrates (CMOS)

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- Automotive-qualified high volume CMOS fab available for pre-processing
    - 150 employees working in 4 shifts
    - Capacity of 70.000 wafer per year
    - Complete CMOS process line plus integrated sensors
    - 0.35  $\mu\text{m}$  CMOS process
  - Customer supplied wafers on request
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## Lithography

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### Coating / Development

Positive resist	0.8 $\mu\text{m}$ to 50 $\mu\text{m}$
Color filters	Red, green, blue (+ transparent), black
Polyimide	Photo sensitive, ca. 10 $\mu\text{m}$
Specialities	Microlenses

### Exposure

Maskaligner	CD = 1 $\mu\text{m}$ , FS overlay 1 $\mu\text{m}$ , Front to backside alignment
Stepper	CD = 0.35 $\mu\text{m}$ , FS overlay = 0,05 $\mu\text{m}$ , Front-to-backside-alignment, Back-to-backside-alignment

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## Isotropic Etching

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### Wet Processes

Metals	Al, TiW, Cu, other materials upon request
Resist stripping	Solvent + IPA, in-situ stripping in ICP @ 50 °C
Wafer cleaning	EKC265, SC1, Piranha

### Gas Phase Etching / Release Etch

Oxide etch	HF gas
Silicon etch	XeF <sub>2</sub>

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### Dry Etching

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RIE	Oxide, nitride, silicon, Ti(N), Al, a-Si (ICP), AZO (ICP), and other materials upon request
DRIE	Silicon, oxide etch insitu, EPD, SOI, BOSCH-process, aspect ratio max: 1 : 20, sidewall angle: $\pm 0.5^\circ$ , ER up to 20 $\mu\text{m}/\text{min}$
Ion milling	Inert, chemically assisted
Resist etching	Ashing in O <sub>2</sub> /CF <sub>4</sub>

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### Films

#### Non-Metals

Plasma deposition, 400 °C	p/n-aSi, a/ $\mu\text{c}$ -Ge, SiO, SiN
ICP (low T < 200 °C)	aSi, SiO (silane / TEOS), SiN, SiC, DLC
Furnace	Wet/Dry oxidation, H <sub>2</sub> high temp anneal
Atomic layer deposition	Al <sub>2</sub> O <sub>3</sub> , Ta <sub>2</sub> O <sub>5</sub> , ZrO <sub>2</sub> , TiO <sub>2</sub>
TCO	Al doped ZnO
Doping	Yes
Evaporation	High-K layers for optical interference filters

#### Metals

Sputtering	Al, Ti(N), TiW, Cu, NiCr, other materials upon request
Evaporation	Cu, W, Ti and many other metals
Electroplating	Cu, Ni, Sn, Au
Atomic layer deposition	TiN, Ru

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### Integration

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Flip chip: chip-to-chip and chip-to-wafer	Manual and automatic
wafer-to-wafer bonding	Direct, SLID

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## Metrology

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Dimensional	SEM (inline + cross-sections), profilometer, AFM
Visual	3D microscope, inspection microscopes, interferometric microscopes
Characterization	Ellipsometer/reflectometer, defect measurement, CD/overlay, sheet resistance, wafer geometry (bow)

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## Packaging

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Dicing	Si, glass
Thinning/polishing	Standard grinding, TAIKO process
Wire bonding	Al, Au, Pd
Standard ceramic packaging	CLCC, DIL, PGA
Chip-on-board	Die-attach, wire-bond, glob-top
Special packages	Available for optical devices, pressure sensors, medical applications, high temperatures (300 °C)

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## Test

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Manual parameter characterization	
Automatic parameter test	
Fully automated device test (mixed signal)	On wafer or in package
Special test equipment	Optical, pressure, IR, MEMS

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## Reliability

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Pull tests	Wire strength
Temperature change chamber	Max: 150 °C in 15 min ... -65 °C in 15 min
HAST chamber	Temperature + 105 °C ... + 142 °C, humidity 75 ... 100 %, Pressure 0.002 ... 0.196 MPa
Pressure chamber	35 mbar ... 150 bar
Temperature storage	Max: 300 °C
Aging and life cycling	Temperature and bias, customer specified

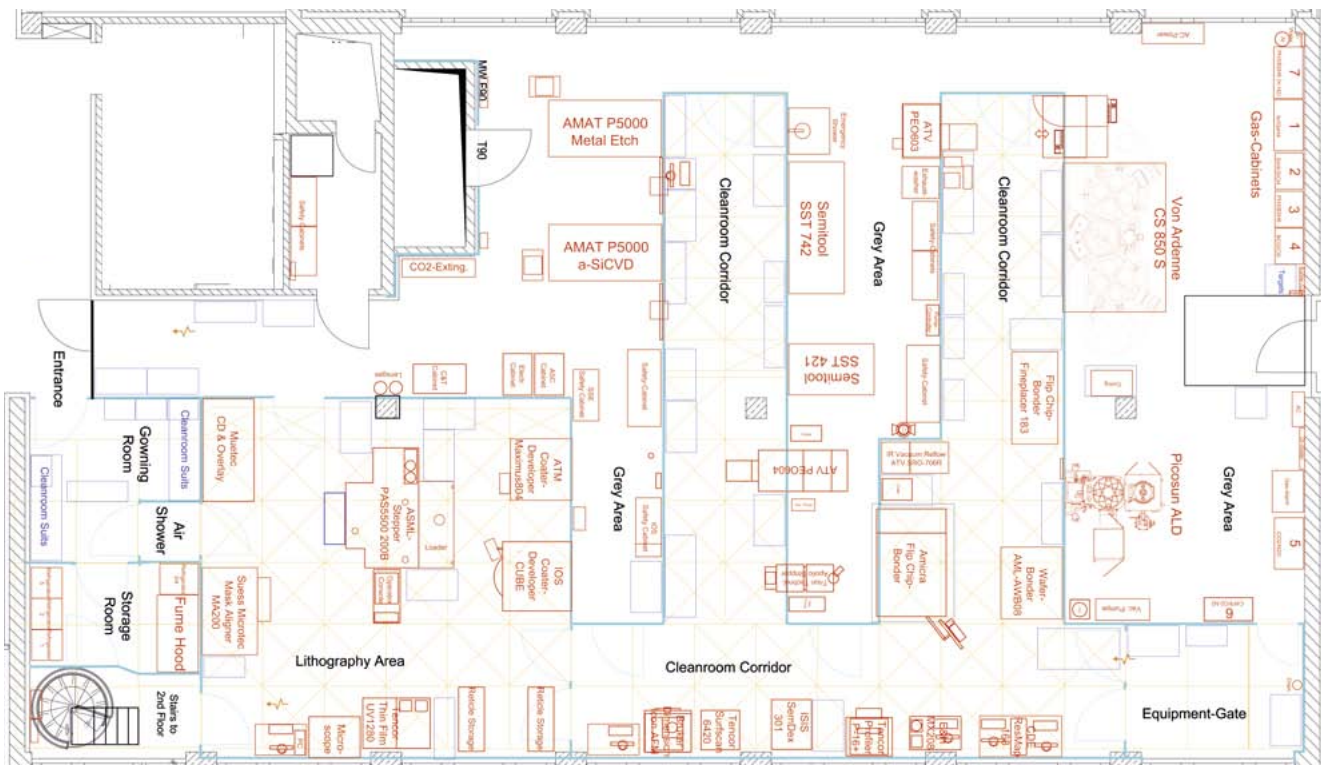


# THE CLEANROOM

The MST Lab&Fab takes up two floors of the Fraunhofer IMS in Duisburg, with a total area of approximately 600 m<sup>2</sup>. The cleanroom has a bay/chase layout with the clean bay area and a chase area containing the equipment bodies, a maintenance area, storage rooms and media supplies. The equipment is installed »through the wall«, minimizing the expensive bay area and still allowing access for maintenance.

## Cleanroom part 1 in the 1. floor

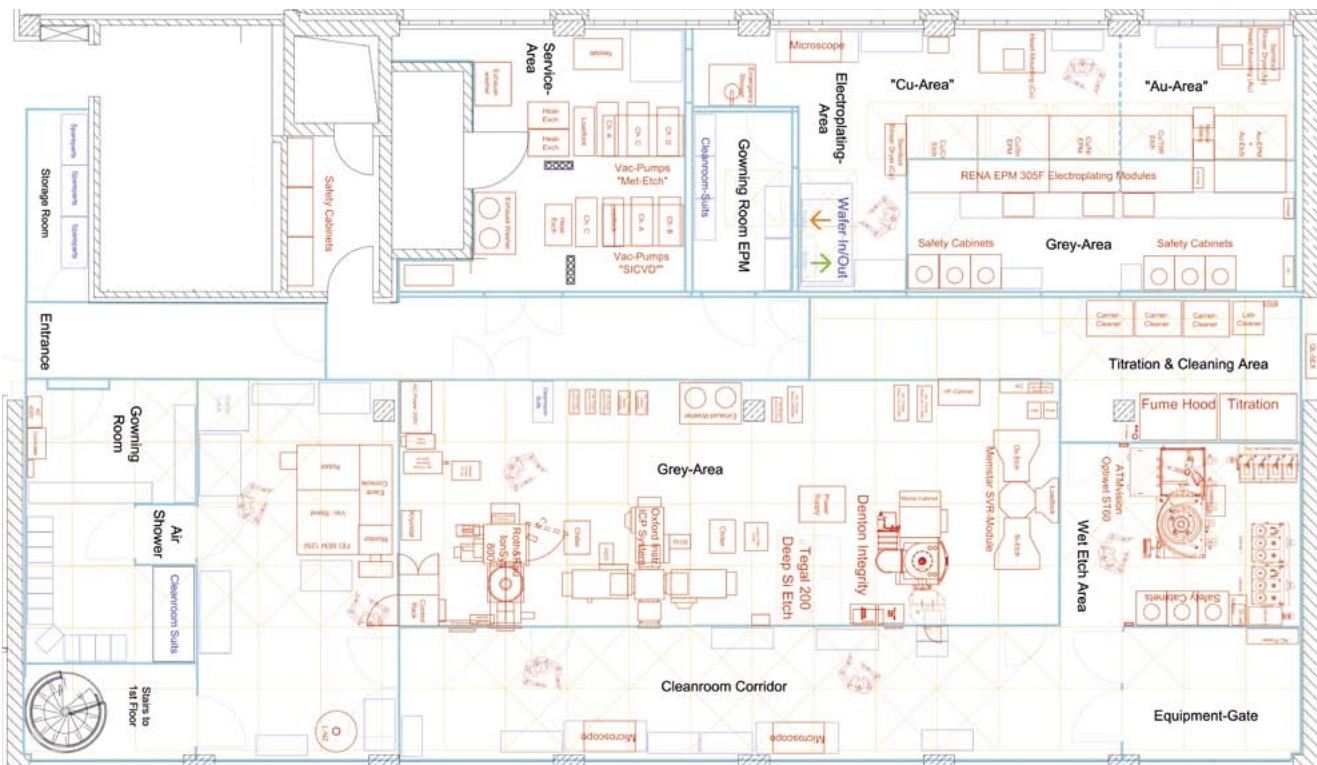
Bay area: approx. 127 m<sup>2</sup> with 110 m<sup>2</sup> in laminar flow for a cleanroom class 3 (DIN EN ISO 14644); the rest of the area is class 5





## Cleanroom part 2 in the 2. floor

Bay area: approx. 130 m<sup>2</sup> with 60 m<sup>2</sup> in laminar flow for a cleanroom class 3 (DIN EN ISO 14644);  
the rest of the area is class 5



# THE EQUIPMENT

The equipment in MST Lab&Fab is automated, cassette-to-cassette and set up for 200 mm wafers. Thus we are compatible to our CMOS fab and other foundries and ready to offer high quality post-processing.

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## Lithography

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Mask Aligner MA200 Compact  
(*Suess MicroTec*)

Mask aligner broadband, g-line, i-line or gh-line exposure  
resolution: 1  $\mu\text{m}$  in contact mode and 3  $\mu\text{m}$  in proximity  
mode, topside (TSA) and bottomside alignment (BSA)

Spin Coater Developer Maximus 804  
(*ATMvision*)

Resist coating and development for positive photoresists  
(0.7 – 25  $\mu\text{m}$ )

Spin Coater Developer Cube Series  
(*IOS Instruments*)

Resist coating and development for coloured positive  
photoresists (RGBpatterns), thick positive photoresists (25  $\mu\text{m}$ ),  
positive polyimides (5 – 20  $\mu\text{m}$ )

I-Line Stepper PAS5500/200B  
(*ASML*)

I-Line wafer-stepper with 365 nm 5x reduction,  
field size 22,0 x 22,0 mm  
resolution: 0,35  $\mu\text{m}$ , NA = 0,48 – 0,60  
3D-align: front-to-backside (FTBA) and back-to-backside  
alignment (BTBA)

Single Wafer Spin Processor WS-400B  
(*Laurell Technologies Corp.*)

Resist coating with new materials

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## Deposition and Etching

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P5000 MxP  
(*Applied Materials*)

Metal-etching, oxide- / nitride-etching

P5000  
(*Applied Materials*)

CVD (doped / undoped silicon oxides and amorphous silicon,  
silicon nitride)

SVR Multisystem with XeF<sub>2</sub> + HF-Modules  
(*Memstar*)

Isotropic silicon and silicon-oxide etching



Deep Plasma Etching System Tegal 200  
(Tegal Corp.)

Anisotropic silicon etching

Ionsys 500  
(Roth & Rau)

Ion beam etching

ALD reactor ALS system  
(Picosun)

Atomic layer deposition with  $\text{Al}_2\text{O}_3$ ,  $\text{Ta}_2\text{O}_5$ ,  $\text{ZrO}_2$ ,  $\text{TiO}_2$ , TiN, Ru

ICP Deposition System 100 Pro  
(Oxford Instruments)

CVD (TEOS-based silicon oxides, -nitrides), oxide-etching

PVD CS850S  
(Von Ardenne Anlagentechnik GmbH)

PVD with targets of Cu, Al, Ti, Cr, Ag, NiCr, TiW, NiV, AlCu, AlSi

Integrity 26 Electron Beam Deposition System  
(Denton Vacuum)

Deposition of optical films (Cu, W, R, Ti, others ...)

Apollo  
(Trion)

Plasma resist stripper,  $\text{O}_2$  /  $\text{CF}_4$

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## Wet Processing

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Spin Rinser Dryer 280S  
(Semitool)

Wafer cleaning

Spray Solvent Tool 742  
(Semitool)

EKC-clean, resist stripping with AZ100/ IPA

Spray Solvent Tool 421  
(Semitool)

Resist stripping

EPM 305F  
(Rena Sondermaschinenbau GmbH)

Electroplating (Au, Cu, Sn, Ni)

Suncup EPM  
(NB Technologies)

Electroplating (tests)



Wet Spin Processor System OPTIwet ST 30  
(ATMvision AG)

Wet etching of Cu, TiW, Al; wafer cleaning  
(Piranha, SC1, Megasonic, DI-Jet)

### Thermal Processing

ATV SRO-706-R  
(ATV Technologie GmbH)

Solder reflow oven

ATV PEO-603  
(ATV Technologie GmbH)

Multipurpose fast ramping process furnace  
(N<sub>2</sub>-atmosphere, vacuum)

ATV PEO-604  
(ATV Technologie GmbH)

Multipurpose fast ramping process furnace  
(N<sub>2</sub> and H<sub>2</sub>-atmosphere, vacuum)

### Bonding Processes

Flipchip Bonder Fineplacer183  
(Finetech GmbH)

Flipchip bonding

High Accuracy Die-Bonder AFC  
(AMICRA Microtechnologies GmbH)

Flipchip bonding

Waferbonder AML-AWB08 Platform  
(Applied Microengineering Ltd.)

Wafer bonding

### Inspection and Measurement

Surface Profiler P-16+  
(KLA Tencor)

Step height measurement

Inline-SEM 1250  
(FEI)

Electron beam microscope, full wafer

CDE Resmap 168  
(CDE)

Sheet resistance measurement



UV-1280 Advanced Thin Film Measurement System  
(KLA Tencor)

Optical thin film measurement

Dimension Icon-PT Scanning Probe Microscope  
(Veeco)

Atomic force microscope

Surfscan 6420 Wafer Surface Analysis System  
(KLA Tencor)

Particle measurement on wafer surfaces

Qualilab QL-5EX  
(ECI Technology)

Programmable system for analysis of organic additives  
and inorganic compounds

Muetec 3000  
(MueTec GmbH)

Optical CD and overlay measurement, inspection

Capacitive Wafer Geometry Measurement  
System MX 208  
(Eichhorn & Hausmann)

Wafer geometry measurement

SEMDEX 301  
(ISIS Sentronics GmbH)

Optical wafer inspection tool

LH Microscope  
(Nikon Metrology GmbH)

Optical wafer inspection tool

3D Konfokal Mikroskop  
(Leica Microsystems)

Optical wafer inspection tool

- 1 *Programming a recipe*
- 2 *Wafer cleaning*
- 3 *Electroplating*

# THE PROCESS MODULES

## Available resources

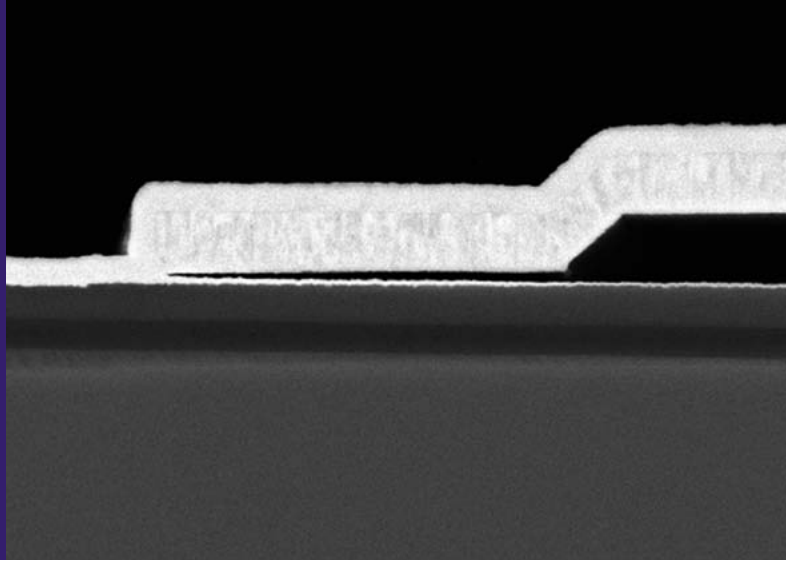
The aforementioned equipment is ready to provide you with individual process steps. Your sensing and actuating devices may require more than that: Process modules, a consolidation of thoroughly grouped process steps, form the basis of our microsystem development. Several modules are described in the following; listing the technologies used naming some of the underlying principles, and their already existing or potential application. Further modules will be added, derived from current projects or adapted to your requirements.

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## Overview Process Modules (8 inch)

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- Free standing structures
- Electrodes
- Packaging
- Optical components and devices
- Bio sensors
- Nanostructures
- Passive components



# FREE STANDING STRUCTURES

Surface micromachining is used to generate freestanding structures. A sacrificial layer is deposited and structured, the functional layer on top will be freed by removing the sacrificial layer underneath.

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## Technologies

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- (SOI-) Free standing structures
- Electrically connected free standing structures a-Si/SiGe/Ge
- Sealed structures
- Sacrificial techniques (oxide, a-Si)

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## Principles

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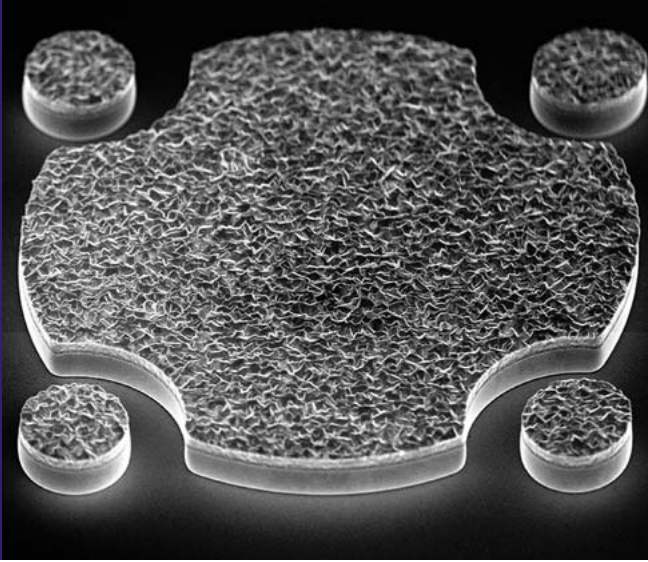
- Thermal isolated structures
- Resonantly oscillating components, e. g. cantilevers, membranes

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## Applications

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- Bolometric sensors
- Fluid flow sensors
- Mass sensor
- Optical devices
- Pressure sensors



# ELECTRODES

Accessing sensitive layers, packaging of sensors, or supplying signals and power require reliable electrodes and contacts. Low resistance and inert metals are deposited and structured, their surfaces sometimes modified by additional thin film coatings.

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## Technologies

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- Substrate planarized CMOS
- Thin film electrodes (sputtering, evaporation, atomic layer deposition)
- 3D-electrodes (electroplating)

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## Sensor Principles

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- Resistive
- Capacitive sensing
- Electrochemical redox reaction

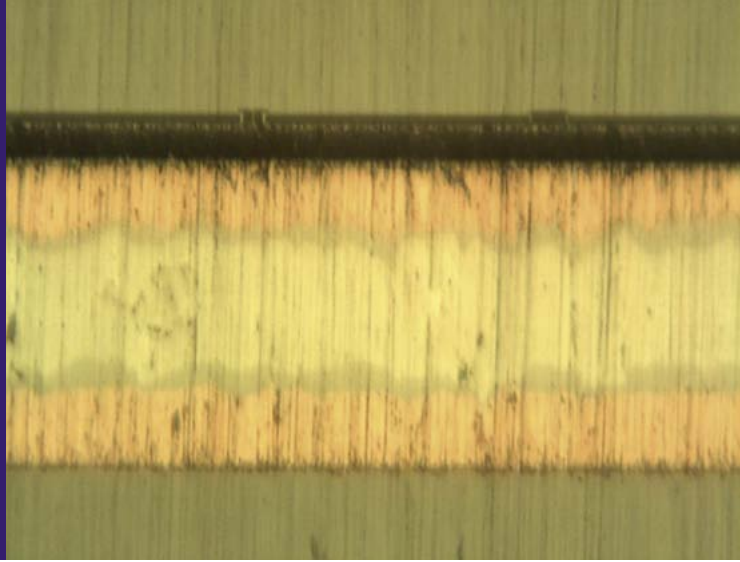
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## Applications

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- Interdigital electrodes
- Electro chemical sensors
- Capacitive and resistive sensors
- Moisture sensor





# PACKAGING

Microsystems packaging is science and art. It combines offering access for the media to be measured with protecting the device for longtime reliable operation.

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## Technologies

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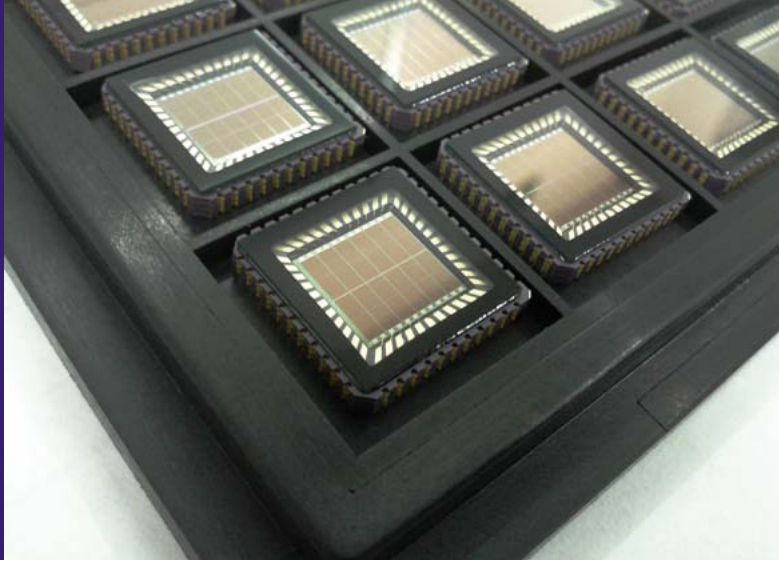
- Wafer-to-wafer bonding (SLID, direct)
- Flip chip bonding
- Wafer thinning
- Electroplating

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## Applications

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- Chip scale packaging
- Vacuum packaging
- High temperature packages
- Flip-chip-to-ceramic package
- Bumping (Au, Ni, Sn, Cu)
- Optically transparent lids
- Anti reflecting coating (from UV to IR)
- Getter



# OPTICAL COMPONENTS AND DEVICES

Semiconductor layers are sensitive to light. If you put them on top of the CMOS wafer, novel imaging applications may be generated. Or you may just modify an existing optical device by adding filters, lenses or light shields. We have already dealt with optical wavelength from extreme UV (10 nm) to infrared ( $> 10 \mu\text{m}$ ).

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## Technologies

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- Anti reflecting coatings/structures evaporation
- Atomic layer deposition
- Micro lenses
- Color filters
- UV transparent passivation
- Hybride imager integration by wafer to wafer bonding

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## Principles

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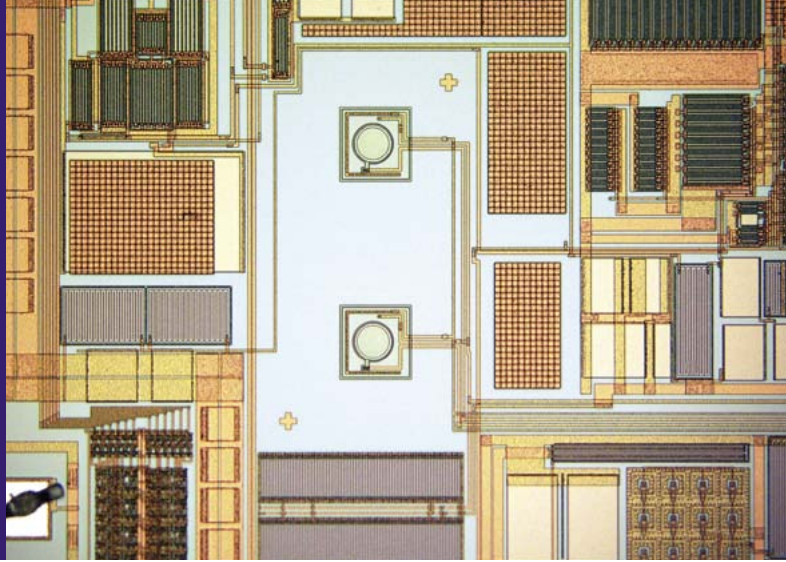
- Optically active layers: Si, SiGe, Ge (amorphous, micro-crystalline)
- Evaporation, ALD
- Interference layers (vis, IR, UV)
- Backside illuminated imagers

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## Applications

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- Photo diodes
- Photo cells
- Imagers (vis, IR, UV)
- Optical components (optical interference filter, Fabry-Pérot filter)



# BIO SENSORS

Postprocessing on CMOS is an ideal means for intelligent bio sensors. If an adsorption reaction of a bio molecule has an electronic response, e. g. a charge change, you may read it out directly. If the adsorption creates a mere mass change, read it out with a resonantly vibrating microstructure. Resistance or capacitance changes, even the local detection of light are other useful sensing methods.

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## Technologies

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- Surface machined membranes
- Surface functionalized electrodes
- 3D electroplated electrodes

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## Principles

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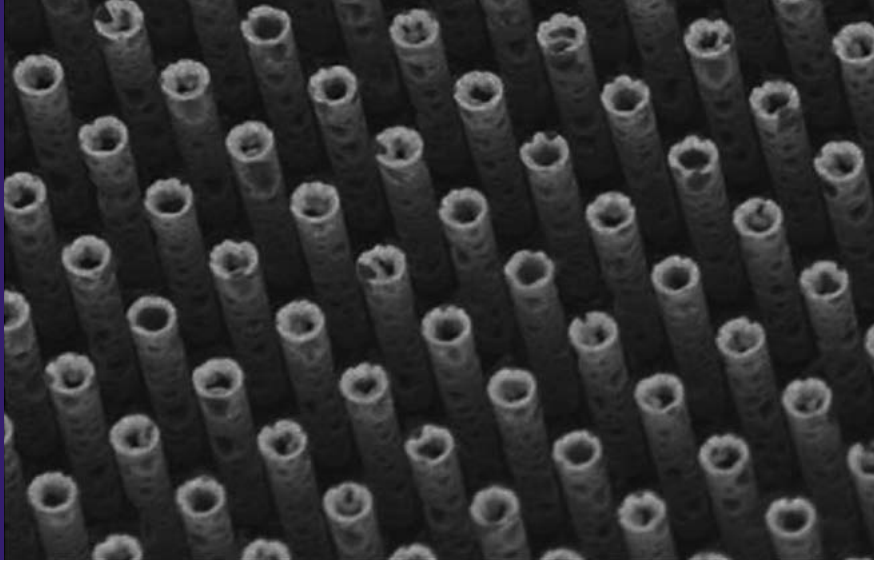
- Resonant components: cantilevers, membranes
- Capacitive sensing
- Electrochemical reactions

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## Applications

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- Glucose sensor
- Allergen sensor
- Nanopotentiostat



# NANOSTRUCTURES

Inert films, a few 10 nm thick, offer excellent device protection, when combined with suitable passivation layers. The exploitation of nanostructured electrodes, especially when combined with CMOS readout or stimulation, has just scratched the surface of potential applications.

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## Technologies

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- Thin protection films by atomic layer deposition
- 2D and 3D nano structures

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## Principles

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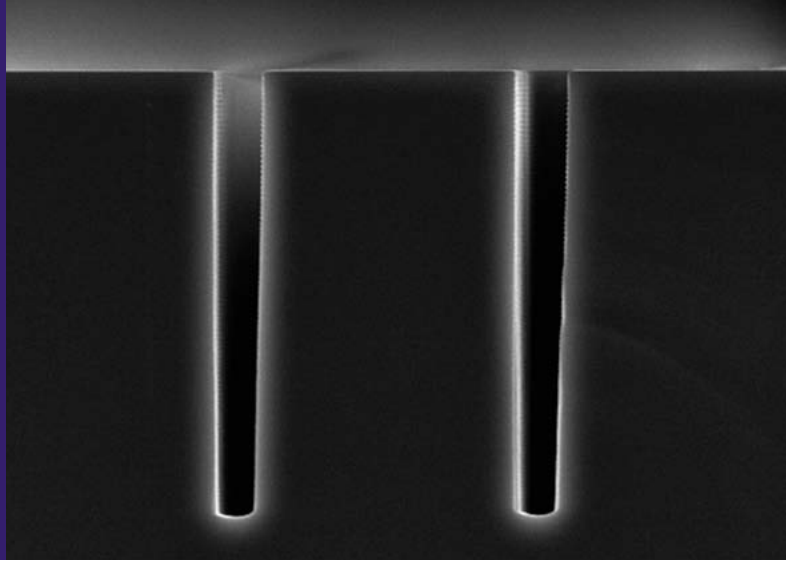
- Protection films
- 3D electrodes

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## Applications

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- Nano needles
- Nanowires
- MOx gas sensors
- Bio-compatible protection layers
- Catalytic layers



## PASSIVE COMPONENTS

Microsystems integration not only requires active devices like sensing layers or circuits, but benefits from passive devices as well. Electronic passive devices (capacitors, resistors) may be integrated or used as standalone components. We may use the process steps available also to create passive mechanical structures, e. g. precision holes, or modified surfaces.

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### Technologies

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- Bulk micromachining
- High aspect-ratio etching
- Atomic layer deposition

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### Applications

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- (High temperature) trench capacitors
- Metal film resistors with near zero TCR
- Oxide isolated trenches in thickfilm SOI
- Sieves

# DIRECTIONS & CONTACT

## Fraunhofer Institute for Microelectronic Circuits and Systems IMS

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### Access by car

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#### via motorway A40

- exit »Duisburg-Kaiserberg«
- direction »Innenstadt«, »Zoo« (Carl-Benz-Straße)
- after approx. 1 km (direction »Innenstadt«) turn right into Mülheimer Straße
- pass the Zoo
- after 300 m turn left at traffic light into the Lotharstraße
- at third street turn right into Finkenstraße
- institute is on the right side

#### via motorway A3

- exit »Duisburg-Wedau«
- direction »Innenstadt« (Koloniestraße)
- at third traffic light turn right into Mozartstraße, which turns into Lotharstraße in the following of the street
- after 800 m turn left into Finkenstraße
- institute is on the right side

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### Access by airplane

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arrival at Airport Düsseldorf-International

- a) Taxi (duration 20 min.)
- b) take the shuttle bus to airport railway station.  
In the following use the train to Duisburg Central Station.

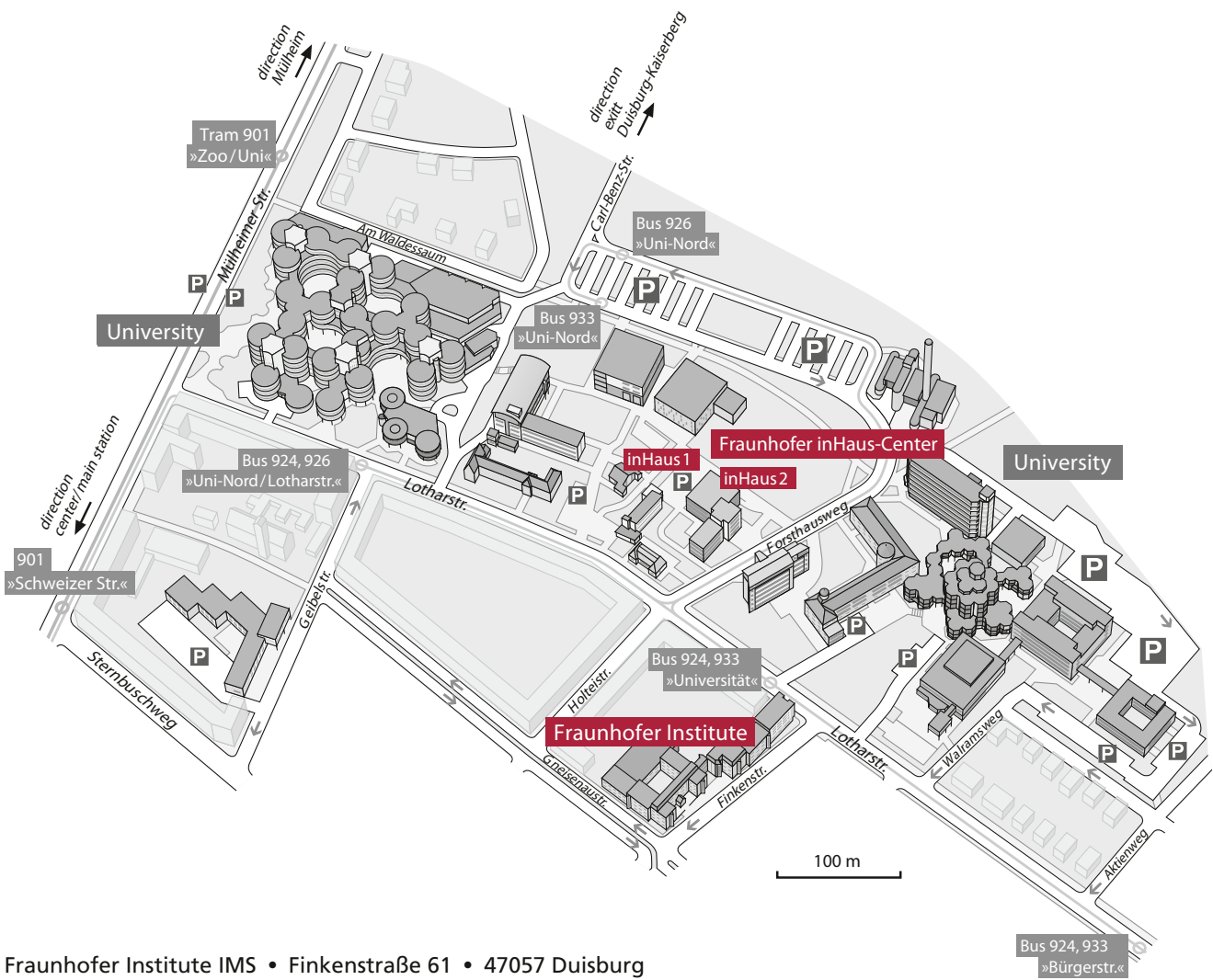
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### Access by train

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arrival Duisburg Central Station

- a) Taxi (duration 5 min.)
- b) Bus number 924 (direction »Sportpark«), exit at station »Universität«, duration about 8 min. Bus number 933 (direction »Universität«). Exit at station »Universität«, duration about 11 min.



Fraunhofer Institute IMS • Finkenstraße 61 • 47057 Duisburg

**Fraunhofer Institute for Microelectronic  
Circuits and Systems, IMS**

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