Fraunhofer IMS

AIRISC - RISC-V Cores for Smart Embedded Sensing

Highly Configurable and Costumizable RISC-V Processor Systems for a Wide Range of Embedded AI Applications

Trustworthy RISC-V Cores

The AIRISC family of RISC-V cores developed by Fraunhofer IMS enables efficient machine learning and AI in sensors, IoT devices, and other embedded applications. AIRISC variants with extended safety mechanisms such as dual-core lock-stepping (DCLS) or error correcting codes (ECC) are available for use in fail-safe systems according to ISO 26262 (up to ASIL-D) and DIN 61508. Because intellectual property protection is very important in these applications, the AIRISC family provides cryptographic security features such as firmware protection and secure booting. The free RISC-V architecture makes it possible to implement customer-specific extensions in a short time and thus provide optimum computing performance for special applications. These features make AIRISC the best choice for real-time embedded sensor applications and integration into IoT systems. **The following application-specific versions of AIRISC are available:**

AIfES

The whole RISC-V family is compatible with our software-framework AIfES®

Find out more: www.aifes.ai

AIRISC-Famliy of RISC-V Cores

Core	Application
AIRISC-POWER	Power module driver and predictive maintenance of machines
AIRISC-LiDAR	Pre-processing of high data-rate LiDAR sensor data
AIRISC-TIMESERIES	On device processing of sensor data
AIRISC-SAFETY	Control systems with ASIL-D requirements

System-on-Chip Design Services

- From concept and feasibility studies to the creation of complete designs and design support
- Mixed signal system design based on RISC-V for smart sensors
- FPGA-based developments and customer-specific ASIC solutions
- Functional safety and cyber security for critical applications in the aerospace, automotive and industrial sectors
- Efficient hardware for inference and training of neural networks

Fraunhofer IMS

Designed for Embedded AI

In interaction with the AIfES software library invented by Fraunhofer IMS, the AIRISC processor family supports the inference and training of neural networks directly on the embedded device. Integrated accelerators enable distributed training in networked devices (federated learning) and also the calibration of sensors using AI. Data processing directly in the sensor, without the need for permanent communication with the cloud, makes the AIRISC processor interesting for energy-autonomous and wearable sensor systems. It enables the design of compact privacy-preserving electronic systems and ISA extensions.

Features

- 32-bit, 5-stage pipeline
- Highly modular: tune area, power, and performance by enabling features in a single central configuration file
- E - reduced register set
- M - single cycle multiplier/divider
- C - compressed instructions
- F - single precision floating point unit (FPU)
- P - SIMD instructions for AI
- Branch prediction and Return Address Stack (RAS)
- Configurable hardware breakpoints/watchpoints
- Hardware support for AIfES embedded AI library

Modules/Peripherals

- AHB-Lite system interface
- GPIO
- UART
- SPI Master/Slave
- Timer
- JTAG
- Dynamic reconfiguration module (on Xilinx 7-series)
- Embedded FPGA module

Deliverables

- RTL Verilog sources
- Verification suite
- Synthesis and P&R scripts for Cadence Genus/Innovus
- Register and module description
- Integration guide
- Example projects for Diligent NexysVideo, CMOD A7 and ArtyA7 boards
- Including Coremark, FreeRTOS-Demo, Peripheral Demo and embedded AI Demo

Contact

Business Unit Industry
sales@ims.fraunhofer.de

Fraunhofer Institute for Microelectronic Circuits and Systems IMS
Finkenstraße 61
47057 Duisburg
www.ims.fraunhofer.de/en.html